IN THE CLAIMS

1. (currently amended) A method for forming a dual damascene structure for a semiconductor device comprising the steps of:

providing conductive regions on a first layer;

forming an interlevel dielectric layer over the first layer;

forming an etch stop layer over the interlevel dielectric layer, the etch stop layer including a polymer material having a dielectric constant of less than about 3.0;

patterning the etch stop layer to form a via pattern;

depositing a trench dielectric layer on the etch stop layer and in holes of the via pattern;

forming trenches in the trench dielectric layer by etching the trench layer in accordance with a trench pattern; and

forming vias in the interlevel dielectric layer by etching through the trenches using the etch stop layer to self-align the trenches to the vias and expose the conductive regions on the first layer, said etching eroding portions of the etch stop layer such that the etch stop layer forms part of the sidewalls of the trenches, thereby improving dielectric strength of the interlevel dielectric layer.

2. (original) The method as recited in claim 1, wherein the polymer includes at least one of polyorylene-ether and polybenzoxazole dielectric.

3. (original) The method as recited in claim 1, wherein the step of providing conductive regions on a first layer includes providing one of metal lines and diffusion

regions.

4. (original) The method as recited in claim 1, further comprising the step of forming a cap layer on the conductive regions to protect the conductive regions from oxidation.

5. (original) The method as recited in claim 1, wherein the interlevel dielectric layer and the trench dielectric layer are comprised of a same material.

6. (original) The method as recited in claim 5, wherein the same material includes one of a nitride and an oxide.

7. (original) The method as recited in claim 1, wherein the interlevel dielectric layer and the trench dielectric layer are selectively etchable relative to the etch stop layer.

8. (original) The method as recited in claim 1, wherein the interlevel dielectric layer and the trench dielectric layer are comprised of a different material.

9. (original) The method as recited in claim 1, wherein the step of patterning the etch stop layer to form a via pattern includes employing a hard mask layer to form the via pattern.

10. (original) The method as recited in claim 1, further comprising the step of depositing conductive material to concurrently form contacts in the vias and conductive lines in the trenches.

11. (original) The method as recited in claim 1, wherein the step of forming an etch stop layer over the interlevel dielectric layer includes spinning on and curing the polymer.

12. (currently amended) The method as recited in claim 1, wherein the etch stop layer ~~includes~~ has a

thickness ~~of between about 100 nm to~~greater than 200 nm and at most about 250 nm.

Claims 13-23 (canceled).

Claims 24-29 (withdrawn).